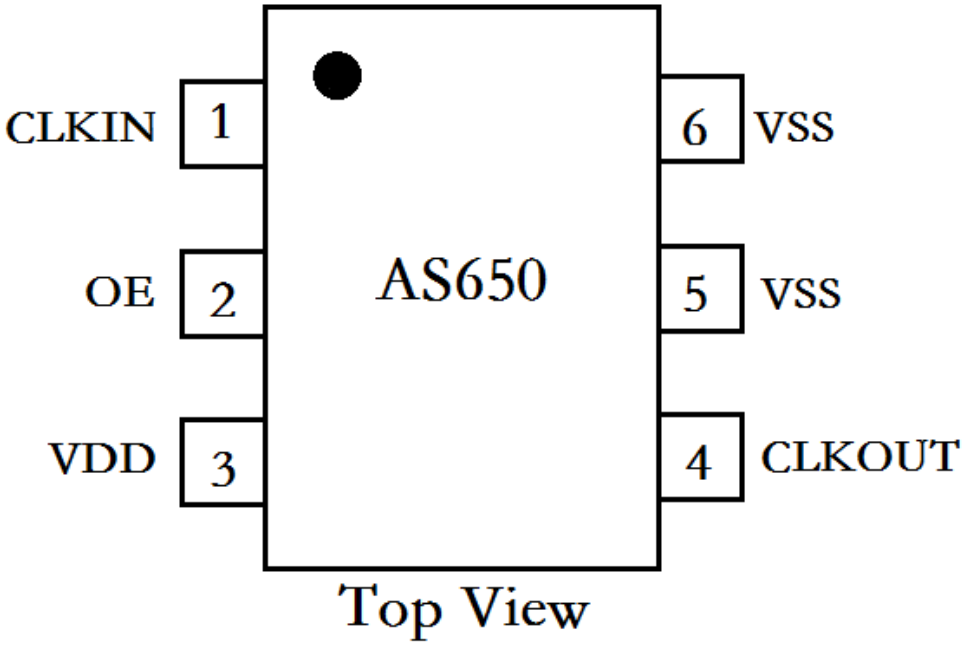
AS650 - Clock Buffer

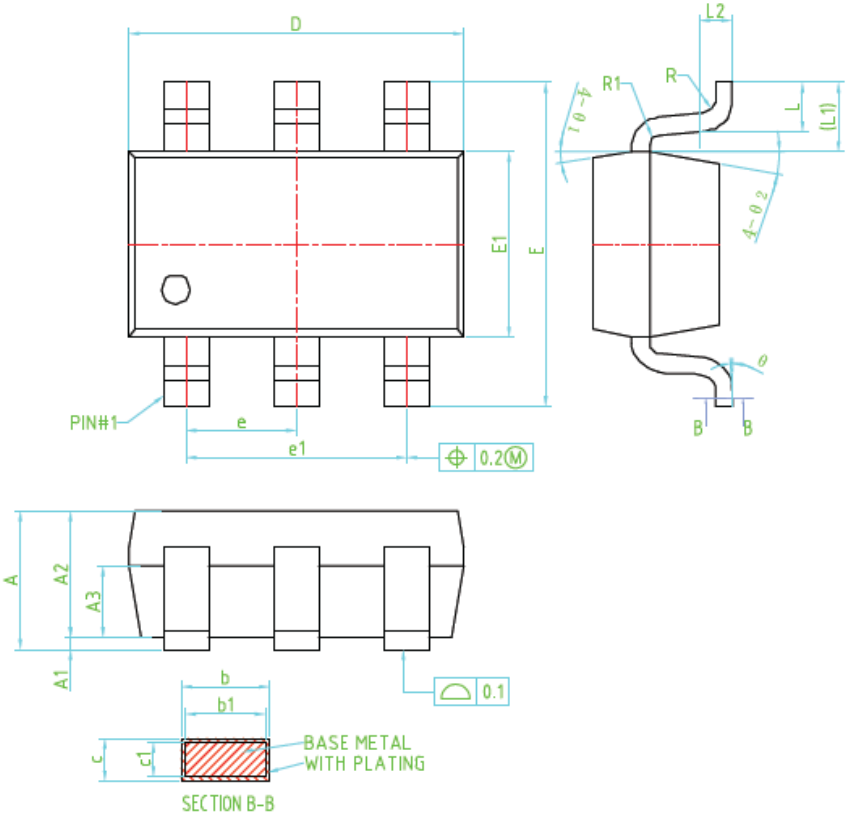
一. Pin Configuration

Pin No	SOT-23 Package	备注
1	CLKIN	10MHz~120MHz AC couple is needed
2	OE	1. OE=VDD: CMOS Output, Fclkout=Fclkin 2. OE=VSS: CLKOUT High Impedance
3	VDD	1.6V~3.6V
4	CLKOUT	CMOS Output Fclkout=Fclkin
5	VSS	GND
6	VSS	GND



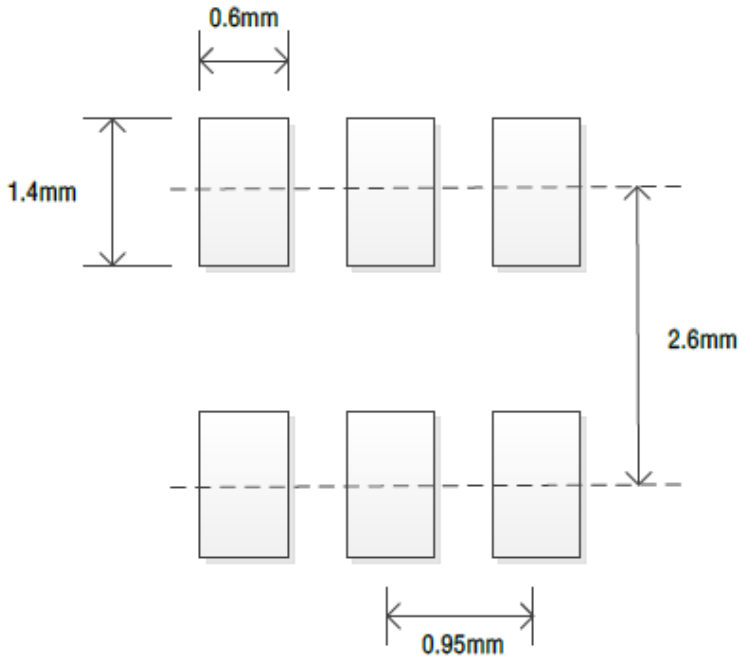
Top View

二. Package Outline Dimensions



COMMON DIMENSIONS(UNITS OF MEASURE MILLMETER)			
SYMBOL	MIN	NOM	MAX
A	–	–	1.25
A1	0	–	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	–	0.50
b1	0.36	0.38	0.45
c	0.14	–	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.6	2.8	3.00
E1	1.526	1.626	1.726
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.35	0.45	0.60
L1	0.59REF		
L2	0.25BSC		
R	0.10	–	–
R1	0.10	–	0.20
θ	0°	–	8°
θ1	3°	5°	7°
θ2	6°	–	14°

三. Layout



Example Board Layout